CLAIMS

What is claimed is:

1. A prescaler circuit for use in a frequency source, comprising an input node for receiving an input signal having a characteristic frequency to be divided, an output node for outputting a frequency divided signal to an output of the frequency source, and at least one divider stage coupled between the input node and the output node for dividing the input signal by a predetermined amount, and further comprising at least one resampling stage for receiving an output signal from said at least one divider stage, and for synchronizing edges of the output signal to edges of the input signal.

2. A phase locked loop comprising a phase comparator generating an output signal that is used to drive a voltage controlled oscillator, and a modulus N prescaler circuit coupled to an output of said voltage controlled oscillator, said prescaler circuit comprising an input node for coupling to said voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N, an output node for outputting a frequency divided signal that is coupled to said phase comparator, and a plurality of divider stages coupled between the input node and the output node for dividing the input signal by N, and further comprising at least one resampling stage coupled to an output of at least one of said divider stages for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby reducing temporal ambiguity in the occurrence of the edges of the output signal.

3. A phase locked loop as in claim 2, wherein the value of N is programmable.

4. A phase locked loop as in claim 2, wherein said at least one resampling stage is comprised of a D-type flip-flop that is clocked with said input signal.

5. A method for reducing power consumption in a frequency source of a mobile station, comprising:

operating a phase locked loop as part of the frequency source to generate a signal having

a desired frequency, the step of operating the phase locked loop including a step of dividing a frequency of an output signal of a voltage controlled oscillator by a predetermined amount; and

resampling the frequency divided signal using the output signal of the voltage controlled oscillator to reduce jitter in the frequency divided signal, without increasing the current consumption of frequency divider circuits that comprise the phase locked loop.

6. A method as in claim 5, wherein the step of resampling operates a modulus N prescaler circuit that is coupled to the output of the voltage controlled oscillator, the prescaler circuit comprising an input node for coupling to the output of the voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N, an output node for outputting a frequency divided signal that is coupled to a phase comparator of the phase locked loop, and a plurality of the frequency divider circuits coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby reducing jitter of the output signal.

7. A method as in claim 6, wherein the value of N is programmable.

8. A method as in claim 6, wherein the at least one resampling stage is comprised of a D-type flip-flop that is clocked with the input signal.

9. A method for operating a phase locked loop as part of the frequency source to generate a signal having a desired frequency, comprising:

operating a multi-modulus prescaler function of the phase locked loop to divide a frequency of an output signal of an oscillator by a predetermined amount; and

resampling the frequency divided signal using the output signal of the oscillator to equalize a delay added in different modes of the multi-modulus prescaler function.

10. A method as in claim 9, wherein the delay is equalized without increasing the current consumption of frequency divider circuits that comprise the phase locked loop.

11. A method as in claim 9, wherein the step of resampling operates a prescaler circuit that is coupled to the output of the oscillator, the prescaler circuit comprising an input node for coupling to the output of the oscillator for receiving an input signal having a characteristic frequency to be divided by N, an output node for outputting a frequency divided signal that is coupled to a phase comparator of the phase locked loop, and a plurality of the frequency divider circuits coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby equalizing the delay added in different modes of the multi-modulus prescaler function..

12. A method as in claim 11, wherein the value of N is programmable.

13. A method as in claim 9, wherein at least one resampling stage of the resampling function is comprised of a D-type flip-flop that is clocked with the input signal.

14. A method as in claim 9, wherein the steps of operating and resampling are performed while a mobile station is tuned to a desired RF frequency channel.

15. A method as in claim 9, wherein the steps of operating and resampling are performed while a mobile station is tuned to a desired RF frequency band.

16. A method as in claim 9, wherein the output frequency of the oscillator is set in accordance with an output of a control device of a mobile station.